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Specification

1. Title of the Invention

Formation of Thin Film Transistor

2. What is claimed is:

A method of forming a thin film transistor comprising the steps of:

forming a semiconductor layer on an insulating substrate;

forming a gate insulating film covering said semiconductor layer thereon;

forming a gate electrode layer on the gate insulating film;

patterning the gate electrode layer;

performing an ion implantation in order to form low concentration impurity regions on said semiconductor layer using said gate electrode layer as a mask;

forming a mask layer covering adjacent regions to said gate electrode layer;

performing an ion implantation to form high concentration impurity regions using the mask layer as a mask; and

forming an interlayer insulating film on the whole surface.

3. Detailed Description of the Invention

[Field for Industrial Use]

The present invention relates to a method of forming a thin film transistor, specifically, to a thin film transistor of which source and drain regions have so-called LDD(Lightly Doped Drain) structure in which low concentration impurity regions are formed at a channel side of high concentration impurity regions.

[Summary of the invention]

According to a method of forming a thin film transistor having so-called LDD structure in the present invention, after patterning of a gate electrode layer, an ion implantation is performed while remaining a gate insulating film in order to form low concentration impurity regions, subsequently, an ion implantation is performed to form high concentration impurity regions using a mask layer covering adjacent regions to the gate electrode layer as a mask, thereby preventing any impurity from diffusing from an interlayer insulating film to low concentration impurity regions.

[Description of the Prior Art]

In order to reduce leak of a thin film transistor, and to increase withstand voltage thereof, it is most suitable that source and drain regions should have so called LDD structure in which low concentration impurity regions are formed at a channel side of high concentration impurity regions.

Fig. 2a and Fig. 2b show cross sectional views of forming a thin film transistor. Initially, a semiconductor layer 22 of required size is formed on an insulating substrate 21, then, a gate electrode layer 24 is formed through a gate insulating film 23 which is over the semiconductor layer 22. The gate electrode layer 24 and the gate insulating film 23 are patterned in a self-aligned manner so that a resist layer 25 is formed to mask the adjacent regions to the gate electrode layer 24. Using the resist layer 25 as a mask, ions are implanted to form high concentration impurity regions. (Fig. 2a)

Next, the resist layer 25 as a mask is removed, followed by ion implantation on the whole surface at a concentration of forming low concentration impurity regions 27. After ion implantation, a PSG film 26 is formed on the whole surface as an interlayer insulating film with small stress to be sodium ion stopper. Then, a thin film transistor is completely formed by annealing. (Fig. 2b)

[Problems the invention intends to solve]

In a thin film transistor having an LDD structure, it is confirmed that characteristics are superior as the concentration of impurity regions 27 of source and drain regions is lower.

On the contrary, in the case that an interlayer insulating film is composed of a PSG film 26, boron is diffused in the low concentration impurity regions 27 so that the impurity concentration comes to be high.

Also, in order to form an interlayer insulating film comprising a CVDSi$O_2$ film and a PSG film using a same CVD apparatus, a small amount of boron is included in the CVDSi$O_2$ film and hence, impurity concentration of the low concentration impurity regions 27 comes to be high in the same way.

Therefore, the present invention intends to solve the above technical problem. It is an object of the present invention to propose a method for forming a thin film transistor to prevent impurity from diffusing from an interlayer insulating film to low concentration impurity regions.

[Means for solving the problem]

In order to achieve the above object, in a method of forming a thin film transistor according to the present invention, a semiconductor layer is

formed on an insulating substrate, and then a gate insulating film is formed to cover the semiconductor layer thereon. As a semiconductor layer, for example, a polysilicon layer can be formed. Then, a gate electrode layer is formed on the gate insulating film, followed by patterning the gate electrode layer. Next, ions are implanted to form low concentration impurity regions on said semiconductor layer using said gate electrode layer as a mask. Then, a mask layer is formed to cover adjacent regions to the gate electrode layer. The mask layer is comprised of resist layer, for example. It is preferable that the gate insulating film is patterned with reflection of the pattern of the mask layer. Ion implantation is performed to form high concentration impurity regions using the mask layer as a mask. Subsequently, the mask layer is removed and a PSG film or the like is formed on the whole surface of the interlayer insulating film, followed by the annealing of impurity diffusing region, and so on.

[Effect]

According to the method of forming a thin film transistor of the present invention, the gate insulating film is not patterned at patterning of the gate electrode layer, but remains at least in adjacent regions to the gate electrode layer to the last. As a result, the gate insulating film is finally remained between the interlayer insulating film and low concentration impurity regions so that the problem of impurity diffusion is solved.

[Embodiment]

The preferable embodiment according to the present invention is explained referring to the drawing.

The present embodiment shows an example of forming n-channel thin film transistor having an LDD structure. Referring to Fig. 1a to Fig. 1e, the present embodiment is explained according to the process as follows.

Firstly, a thin film polysilicon layer 2 which is formed on an insulating substrate 1 is conducted by patterning in a required size to form a device region. Then, the polysilicon layer 2 is covered with a gate insulating film 3. The thickness of the polysilicon layer 2 is about 400Å, and the thickness of the gate insulating film 3 is about 500Å.

Then, as shown in Fig. 1a, a gate electrode layer 4 comprising the polysilicon layer is formed on the whole surface and conducted by patterning to be a required size of the gate length and the gate width. The patterning is conducted by using the anisotropic etching having selectivity insulating film and silicon. Therefore, the gate insulating film 3 under the gate electrode layer 4 is not conducted by patterning.

After the patterning of the gate electrode layer 4. using the patterned gate electrode layer 4 as a mask. an ion implantation is conducted to form low concentration impurity regions 5 on the whole surface. Impurities are implanted at a low concentration into the regions of the polysilicon layer 2 not under the gate electrode layer 4. The condition of the ion implantation is 70keV. approximately $1 \times 10^{13} cm^{-2}$. finally. the impurity concentration of low concentration impurity regions 5 is about $1 \times 10^{16}$ - $1 \times 10^{17} cm^{-3}$.

Then. as shown in Fig. 1b. a mask layer 6 covering the adjacent regions 7 to said gate electrode layer 4 is formed. The mask layer 6 is made of, for example photo resist. In this embodiment, the adjacent regions are the regions wherein high concentration impurity regions of source and drain regions are offset from the channel forming region, which remain as low concentration impurity regions 5 in the polysilicon layer 2.

Then, as shown in Fig. 1c, the gate insulating film 3 is performed by anisotropic etching using the mask layer 5. Then, the gate insulating film 3 is removed on the parts excluding the part immediately below the gate electrode layer 4 and the adjacent regions 7 under the mask layer 6, thereby exposing the polysilicon layer 2. In this way, it is preferable to remove the portions of the gate insulating film 3 on high concentration impurity regions in the case of using ion implantation in a high concentration.

Next, as shown in Fig. 1d, ions are implanted to form high concentration impurity regions 8 using said mask layer 6 as a mask. The condition of the ion implantation is, for example 40keV, $2 \times 10^{15} cm^{-2}$. By this ion implantation, high concentration impurity regions 8 to be source and drain regions are formed on the polysilicon layer 2 excluding the part immediately below the gate electrode layer 4 and the adjacent regions 7.

Then, as shown in Fig. 1e, the mask layer 6 is removed, following which a PSG film 9, which is an interlayer insulating film. is formed on the whole surface. Since the gate insulating film 3 is formed on the low concentration impurity regions 5 of the adjacent regions 7, the PSG film 9 is not directly connected with the low concentration impurity regions 5. Accordingly, boron or the like may be prevented from diffusing. Subsequently, a thin film transistor is formed by annealing of source and drain regions, formation of contact holes and a wiring layer, and so on.

In this method of forming a thin film transistor according to the present embodiment, the gate insulating film is not patterned by using the gate electrode layer and self-aligned manner. but the gate insulating film 3 is

extended to the adjacent regions 7 to the gate electrode layer by using the mask layer 6. Because of this, an impurity such as boron may be prevented from diffusing from the interlayer insulating film (PSG film 9) to low concentration impurity regions 5, thereby, preventing variation of the device characteristic. Also, because the surface of low concentration impurity regions 5 is covered with the gate insulating film 3, the interfacial characteristic becomes good. Further, in the case of forming the interlayer insulating film by combination of a CVD$SiO_2$ film and a PSG film, since the gate insulating film 3 is extended to the low concentration impurity regions 5, it is possible to deal with formation process by using same CVD apparatus even if some boron are included in the CVD$SiO_2$ film.

[The Effect of the Invention]

In accordance with the method of forming a thin film transistor in the present invention, the gate insulating film is not patterned when the gate electrode layer is performed by patterning, but at least remains to the last in the adjacent regions to the gate electrode layer. Accordingly, the impurity can be prevented from diffusing from the interlayer insulating film to the source and drain low concentration impurity regions. Also, it is possible to achieve fine interfacial characteristic.

4. Brief Description of the Drawings

Fig. la to le show cross sectional views of the process for explaining an example of formation method of a thin film transistor in accordance with the present invention. Fig. 2a and Fig. 2b show cross sectional views for explaining an example of conventional formation method of a thin film transistor.

1 - - - insulating substrate
2 - - - polysilicon layer
3 - - - gate insulating film
4 - - - gate electrode layer
5 - - - low concentration impurity regions
6 - - - mask layer
7 - - - adjacent region
8 - - - high concentration impurity regions
9 - - - PSG film

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